

MEMORY STRATEGIES INTERNATIONAL TRAINING SEMINARS

www.memorystrategies.com

Lecturer: Betty Prince, Ph.D.

Author of: *Emerging Memories: Technologies and Trends*, 2002, Kluwer Academic
High Performance Memories, Revised Edition 1999, John Wiley & Sons
Semiconductor Memories, 2nd Edition, 1992, John Wiley & Sons

COURSES OFFERED: (DETAILED AGENDAS FOLLOW)

1. MODERN AND EMERGING MEMORIES
2. A BASIC COURSE IN SEMICONDUCTOR MEMORIES
3. OVERVIEW OF EMERGING MEMORIES: TECHNOLOGIES AND APPLICATIONS
4. HIGH PERFORMANCE DRAMS
5. FLASH MEMORIES AND EMBEDDED FLASH
6. MEMORIES FOR PORTABLE SYSTEMS
7. EMBEDDED MEMORIES: DRAM AND FLASH
8. BASICS OF MEMORIES WITH OVERVIEW OF FAST DRAMS
9. BASICS OF MEMORIES AND OVERVIEW OF FLASH
10. BASICS OF MEMORIES WITH OVERVIEW OF FAST SRAMS
11. APPLICATION SPECIFIC AND EMBEDDED DRAMS

1. Seminar on Modern and Emerging Memories

Overview: This two day seminar provides an overview of modern and emerging memories. Modern memories include: high speed DRAMs, low power DRAMs, P-SRAMs, fast SRAMs and NAND / AND and NOR Flash. It also covers emerging memories including: FeRAM and MRAM technology, product status and target applications; after DRAM memories such as SESO, STTM and Capacitorless DRAM: after Flash memories such as silicon nanocrystal and varieties of SONOS; phase change memories such as PCRAM and PMC; negative resistance memories such as T-RAM, non-silicon memories such as molecular memories, and polymer memories along with other vertical memories.

Day 1

- 9:00 Modern DRAMs (Fast, Low Power, P-SRAM)
- 10:30 Fast SRAMs (products and issues)
- 11:00 Post-DRAM Emerging Memories (SESO, STTM, Capacitorless DRAM)
- 12:00 Lunch Break
- 1:00 Modern Flash (NAND/AND, NOR)
- 3:00 Post-Flash Emerging Memories (Silicon Nanocrystal, SONOS)
- 3:45 Polymer Memories
- 4:30 End

Day 2

- 9:00 FeRAM - technology, product status and target applications
- 11:00 Phase Change/Chalcogenide Memory (PMC, PC-RAM)
- 12:00 Lunch Break
- 1:00 Magnetic RAM - technology, product status and target applications
- 3:00 Negative Resistance and Non-Silicon Memory (T-RAM, Molecular)
- 3:45 Vertical Memories
- 4:30 End

2. A BASIC COURSE IN SEMICONDUCTOR MEMORIES

Overview: This two day seminar, targeted at memory marketing staff, managers and new memory engineers, covers the basics of semiconductor memories including markets, applications, process technology, product characteristics, design, test, packaging, and reliability. Products discussed include: Fast DRAMs, Low Power DRAMs, SRAMs, P-SRAMs, Non-Volatile Memories (ROMs, EPROMs, EEPROMs, Flash), an overview of new non-volatiles (FeRAM and MRAM) and embedded memories. The intent is to provide familiarity with most aspects of semiconductor memories.

Day 1:

- 9:00 Memory Market Overview and Applications
- 10:00 Basic Memory Manufacturing Process
- 11:00 Basic Memory Architecture and Cell
- 12:00 Lunch break
- 1:00 Fast SRAM Trends (SRAM, SSRAM, QDR, DDR SRAM, eSRAM)
- 3:00 RAM Reliability Issues (SER, hard errors, leakage, etc.)
- 3:45 Memory Electrical and Test Issues (ECC, BIST, redundancy, repair)
- 4:30 End

Day 2:

- 9:00 DRAM Applications and System Issues
- 9:30 Basics of Fast DRAMs (Operation, Bandwidth, Banking, Page and Burst Mode)
- 10:00 High Performance DRAMs (SDRAM, DDR, DDR2, RDRAM, RL-DRAM)
- 11:00 Low Power DRAMs (FCRAM, MoBL RAM, Cellular RAM, various P-SRAMs, etc.)
- 12:00 Lunch break
- 1:00 Non-Volatiles (EPROM, EEPROM, NAND / NOR Flash, Multi-bit Flash, SONOS / NROM)
- 3:00 New Non-Volatiles (FeRAM, MRAM)
- 3:45 Embedded Memory vs. Advanced Packaging (MCP)
- 4:30 End

3. OVERVIEW OF EMERGING MEMORIES: TECHNOLOGIES AND APPLICATIONS

Our one-day seminar on Emerging Memories is available as an added day to other seminars. It describes the technology and potential applications of various new memory technologies being investigated in research and development groups today. These are technologies beyond direct evolutionary scaling of CMOS memory technologies used in volume production today.

An agenda for the seminar follows.

Emerging Memories: Technology and Application

9:00 Ferroelectric Memories (2T2C, 1T1C, Materials, Reliability, Trends)

10:30 Magnetic RAMs (Spin Valve, Pseudo-Spin Valve, MTJ, Hall MRAM, Vertical MRAM, Technology, Reliability, Trends)

12:00 Lunch Break

1:00 Non-Volatiles after Floating Gate - Some Contenders
(SONOS/NROM, Proton, Single Electron, Silicon Nanocrystal)

1:45 After DRAM - Some Novel Contenders (Gain memories- SESO, PLEDM, SOI, RTD memories - Esaki RAM, Thyristor RAM, etc.)

2:45 Memories After Silicon
(Polymer, Molecular, Chalcogenic/Ovonic, Carbon Nanotube, Photonic, DNA, etc.)

3:30 Silicon Structure Memories (Micromechanical, Vertical, 3-D, etc.)

4:00 End

4. HIGH PERFORMANCE DRAMS

Overview: This two-day course in High Performance DRAMs provides background for new DRAM engineers and a refresher for current memory Engineering Staff. It focuses on the architecture, operation and applications of the fast new architecture DRAMs. Included are a review of fast access modes Fast Page and EDO, background on the architecture and operation of the various Synchronous DRAMs including SDRAM, DDR SDRAM; Rambus DRAMs; alternative architecture DRAMs such as the CDRAM, ESDRAM, MDRAM, FCRAM and VCDRAM; and the various Graphics DRAMs. DRAM modules, test, and reliability are also covered.

Day 1:

- 9:00 Overview of Fast DRAM System Trends
- 10:00 Basics of fast DRAMs (architecture, bandwidth, granularity, refresh)
- 11:00 Fast access modes in DRAMs (Fast Page, EDO)
- 12:00 Lunch Break
- 1:00 SDR SDRAM Operation
- 2:30 DDR SDRAM Operation
- 3:00 DDR II SDRAM Operation
- 3:30 High Speed Interfaces for DRAMs
- 4:00 Fast Interface DRAMs (RDRAM)
- 4:30 End

Day 2:

- 9:00 Fast Core SDRAM Concepts: (ESDRAM, FCRAM, RL-DRAM, multi-bank DRAM)
- 10:30 Graphics DRAM Issues
- 11:00 Networking DRAMs (1 transistor SRAMs)
- 12:00 Lunch Break
- 1:00 Mobile DRAM/ Low Power DRAM Issues
- 2:00 Fast DRAM Packaging and Modules
- 3:30 DRAM Test and Reliability Issues
- 4:30 End

5. FLASH MEMORIES AND EMBEDDED FLASH: Application, Product and Technology

Overview: This two-day seminar is targeted at engineering staff and management and new non-volatile memory engineers. The first day includes: market and applications for non-volatile memories, an overview of CMOS non-volatile process technology, discussion of products such as NOR and NAND flash memory and alternative flash technologies such as multilevel storage flash and SONOS/NROM types of memories. An overview is given of test and reliability of non-volatile memories followed by of various flash roadmaps. The second day includes: embedded flash applications and systems trends, embedded non-volatile technologies and foundries, new non-volatiles such as FeRAM and MRAM technologies and products and an overview of flash vendors. A discussion of packaging trends including stacked packages, CSP and flipchip is followed by a section on CSP assembly and one on modules and memory cards.

Day 1

- 9:00 Flash Memory Applications, Systems and Markets
- 10:00 Basic CMOS Non-Volatile Processes and Cells
- 11:00 Standalone NOR Flash
- 12:00 Lunch
- 1:00 Standalone NAND Flash
- 2:00 Alternative Flash Technologies (multi-level, SONOS/NROM)
- 3:00 Flash Test and Reliability
- 4:00 Flash Roadmaps
- 4:30 End

Day 2

- 9:00 eFlash Market, Applications and System Trends
- 10:00 Embedded Non-Volatile Technologies and Foundries
- 11:30 New Non-Volatile Products (FeRAM, MRAM)
- 12:30 Lunch Break
- 1:30 Overview of Flash from Various Vendors
- 2:30 Packaging and Package Integration Trends
- 3:30 CSP Assembly Trends
- 4:00 Modules and Memory Cards
- 4:30 End

6. MEMORIES FOR PORTABLE SYSTEMS

Overview: This two day seminar, targeted at portable system application engineers, memory marketing staff, managers and new memory engineers, covers the requirements of memories for portable systems including: processors used in portable systems, trends in low power DRAMs and SRAMs, and low power DRAM architecture and design concepts. Reliability issues such as soft errors at low voltages and atomic particles are discussed. The architecture and operation of various Flash memories used in portable systems are discussed along with basics of the new ferroelectric and magnetic memories being targeted at portable applications. Miniature packaging and modules are also discussed along with an overview of smart cards and memory cards

Day 1

- 9:00 RAM Memory Requirements for Portable Systems
- 9:45 Processors for Portable Systems
- 10:15 Low Power SRAM Trends
- 11:00 Low Power DRAM Trends
- 12:00 Lunch Break
- 1:00 Low Power DRAM Architecture and Design Concepts
- 3:00 Low Voltage Issues for Portable Memory Systems
- 3:30 Reliability Issues for Portable Memories
- 4:30 End

Day 2

- 9:00 Non-Volatile Memory Requirements for Portable Systems
- 10:00 NOR-Flash Architecture and Operation
- 11:15 NAND-Flash Architecture and Operation
- 12:00 Lunch Break
- 1:00 The New Non-volatiles - FeRAM Products and Issues
- 1:45 The New Non-volatiles - MRAM Products and Issues
- 2:30 Other New Non-Volatiles - OUM, Polymer, etc.
- 3:00 Miniature and Modular Packaging (BGA, uBGA, MCM, MCP, Vertical)
- 4:00 Smart Cards and Memory Cards
- 4:30 End

7. EMBEDDED MEMORIES: DRAM AND FLASH

Overview: This two-day seminar is targeted at memory and ASIC engineering staff and management. It covers system problems solved by Integrated Memory/Logic along with some cost analysis, alternatives to integration, and trade-offs along with types of applications most likely to be integrated. Discussion of the technical challenges of integration includes process options, design options (tools, cell and block compilers, macro's, outside design houses) and foundry considerations. Test issues, including BIST and BISR, are considered. Commercial test tools are reviewed. An overview analysis is given of the features and technology of Integrated Memory-Logic chips from various manufacturers.

Day One:

- 9:00 Overview of Trends in Embedded Memory
- 9:30 System Problems Solved by Integrated Memory-Logic
- 10:30 Applications most likely to be Embedded
- 12:00 Lunch Break
- 1:00 Technology Issues - RAM
- 2:00 Technology Issues - Flash
- 3:00 Cost Models and Trade-offs
- 4:00 The Business Model (Foundries, IP, etc.)
- 4:30 End

Day Two:

- 9:00 Design Issues I (architecture)
- 10:30 Design Issues II (compilers, tools, design houses)
- 12:00 Lunch Break
- 1:00 Testing Issues (BIST, Burn-in, BISR, commercial test tools)
- 2:00 Alternatives to Integration (MCM, MCP, etc.)
- 3:00 Analysis of Integrated Chips from Various Manufacturers
- 4:30 End

8. BASICS OF MEMORIES WITH OVERVIEW OF FAST DRAMS

Overview: This two-day seminar is targeted at fast DRAM engineering staff, management and new DRAM engineers. The first day covers the basics of semiconductor memories including markets, applications, process technology, product characteristics, design, test, packaging, and reliability. The second day provides an overview of the fast new architecture DRAMs, their architecture, operation, and application.

Day 1:

- 9:00 Overview of Memory Market and Applications
- 9:45 Basic Memory Manufacturing Process
- 10:45 Basic Memory Architecture and Cell (DRAM, SRAM, Flash)
- 12:00 Lunch break
- 1:00 Fast SRAM Trends (SRAM, SSRAM, QDR, SigmaRAM, DDR SRAM)
- 1:45 Non-Volatile Memory (EPROM, EEPROM, Flash, MRAM, FRAM)
- 2:30 Basics of Integrated DRAM and Logic
- 3:15 Memory Packaging (MCM, MCP, Vertical, Flipchip)
- 4:00 Memory Test and Reliability
- 4:30 End

Day 2:

- 9:00 Fast DRAM Architecture and Operation (basics, FP, EDO)
- 9:45 Basics of Synchronous DRAMs
- 10:30 DDR Basics and Operation
- 11:15 DDR II Basics and Operation
- 12:00 Lunch Break
- 1:00 Application Specific DRAMs (RL-DRAM, FCRAM, ESDRAM, 1T SRAM, RDRAM)
- 2:40 Graphics Memory Issues and Applications
- 3:40 Fast DRAM Modules
- 4:30 End

9. BASICS OF MEMORIES AND OVERVIEW OF FLASH

Overview: This two-day seminar is targeted at engineering staff, management and new engineers involved in the Flash memory or other non-volatile memory areas. The first day covers the basics of semiconductor memories including markets, applications, process technology, product characteristics, design, test, packaging, and reliability. The second day provides an overview of the non-volatile floating gate memories including Flash memories and EEPROMs - their applications, technology, cell structure, architecture, and operation. Embedded Flash options along with Ferro-electric RAMs and other specialty non-volatile memories are also discussed.

Day 1:

- 9:00 Memory Market Overview and Applications
- 10:00 Memory Manufacturing Process
- 11:00 MOS Memory Architecture – Basics of SRAM, DRAM, Non-Volatiles
- 12:00 Lunch break
- 1:00 SRAMs and Cache Theory
- 2:00 Fast DRAM Overview
- 2:30 Basics of Integrated Memory and Logic
- 3:15 Memory Packaging and Assembly Basics
- 4:00 Memory Test and Reliability
- 4:30 End

Day 2:

- 9:00 Flash Memory Applications and Market
- 10:00 Basic CMOS Non-Volatile Processes and Cells
- 11:00 Overview of Standalone Flash Memory - NOR Flash
- 12:00 Lunch
- 1:00 Overview of Standalone Flash Memory - NAND Flash
- 2:00 Embedded Flash - technology and cell
- 2:45 Alternative non-volatile technologies (FRAM, MRAM)
- 3:30 Flash Test and Reliability
- 4:00 Flash Modules and Memory Cards
- 4:30 End

10. BASICS OF MEMORIES WITH OVERVIEW OF FAST SRAMS

Overview: This two-day seminar is targeted at engineering staff, management and new engineers involved in the SRAM area. The first day covers the basics of semiconductor memories including markets, applications, process technology, product characteristics, design, test, packaging, and reliability. The second day provides an overview of SRAMs, their architecture, technology, operation, application, test, and packaging. Embedded SRAMs are also discussed.

Day 1:

- 9:00 Memory Market Overview and Trends
- 9:30 Applications for Memories – Markets and Systems
- 10:15 Memory Manufacturing Process
- 11:00 MOS Memory Architecture
- 12:00 Lunch break
- 1:00 Non-volatile Memory Overview
- 2:00 Modern DRAM Overview
- 3:00 Basics of Integrated Memory and Logic
- 4:30 End

Day 2:

- 8:30 SRAM Applications and Trends
- 9:45 Basics of SRAM Architecture
- 10:15 Asynchronous SRAMs
- 11:15 Cache Theory
- 12:00 Lunch Break
- 1:00 Synchronous SRAMS
- 2:00 Specialty and Embedded SRAMs
- 3:00 Memory Packaging and Assembly Basics
- 3:45 Memory Test and Reliability
- 4:30 End

11. APPLICATIONS SPECIFIC AND EMBEDDED DRAMS

Overview: This two-day course is covers commodity DRAMs, Applications Specific DRAMs and Embedded DRAMs. It is targeted at engineering management, staff and new DRAM and ASIC DRAM engineers. It provides an overview of the high performance DRAMs, their architecture, operation, and application. Included are a review of fast access modes in DRAMS including SDR SDRAM, DDR & DDR II SDRAMs; Rambus DRAMs; fast core DRAMs such as the ESDRAM, 1-Transistor SRAMs, FCRAM, and RL-DRAM. High-speed interfaces, modules, test, and reliability are also covered. The second day covers systems problems solved by Integrated RAM-Logic along with consideration of the types of applications most likely to be integrated. Discussion of the technical challenges of integration includes various process options, design considerations, and design tools. Test issues, including BIST and BISR, are considered and commercial test tools are reviewed. An overview analysis is given of the features and technology of Integrated RAM-Logic chips from various manufacturers.

Day 1:

- 9:00 Overview of Fast DRAM System Trends
- 9:30 Basics of fast DRAMs (architecture, bandwidth, granularity, refresh, access modes)
- 10:15 SDR SDRAM Basics and Operation
- 11:30 DDR SDRAM Basics and Operation
- 12:00 Lunch Break
- 1:00 DDR II SDRAM Basics and Operation
- 2:00 High Speed Interfaces
- 2:30 Alternative Architecture DRAMs (Including Networking and Graphics DRAMs and Packet Protocol DRAMs)
- 3:15 DRAM Test and Reliability Issues
- 4:00 Packaging and Module Issues
- 4:30 End

Day 2:

- 9:00 Analysis of Market and Trends in Embedded DRAMS
- 9:30 System Problems Solved by Embedded DRAM
- 10:15 Embedded DRAM Applications - Solutions and Trade-offs
- 11:00 Embedded DRAM Architecture and Trends
- 12:00 Lunch Break
- 1:00 Technology Issues (process options, cell types, performance, power, refresh)
- 1:45 Design Issues (compilers and design tools, bandwidth and power, parallelism)
- 2:30 Supplier Models - ASIC, Custom DRAM, Foundries
- 3:15 Testing Issues (BIST, Burn-in, repair, commercial test tools)
- 4:00 Alternatives to Integration (MCM, CSP, MCP)
- 4:30 End

Contact: Memory Strategies International
16900 Stockton Drive
Leander, Texas 78641

Phone: 1-512-260-8226
FAX: 1-512-260-3967
info@memorystrategies.com
www.memorystrategies.com

Cost:

2-Day Course: \$2600.00 per course up to 10 participants. This base fee is due in advance.
\$250.00 for each additional participant over 10, with maximum of 30 per course.
1-Day Courses are only offered in combination with other courses. Contact us for information.

A binder of the lecture material is provided to each participant. Lecture room and digital projector are to be provided by sponsoring organization. Travel expenses for one from Austin, Texas are additional. Attendance numbers must be provided 10 days in advance.

Cancellation Policy: Cancellations less than 30 days in advance will be billed for any non-refundable travel arrangement expenses. To cover preparation costs, cancellations less than 10 days in advance will be billed a fee of \$60 per person per course. (41 days & 20 days, respectively, for classes outside the continental U.S.)

Lecturer:

Dr. Prince is CEO of Memory Strategies International, a semiconductor memory services company in Leander, Texas, founded in 1993 and President of Processor Strategies International, a subsidiary of Memory Strategies. She has spent over 30 years in Engineering, Marketing and Operations Management in the semiconductor industry in both the USA and Europe with Texas Instruments, N.V. Philips, Motorola, RCA Semiconductor, and Fairchild Semiconductor.

She is on the Scientific Advisory Board of Cavendish Kinetics (S'Hertogenbosch, NL), and has also served on the Scientific Advisory Boards of Silicon Access Networks (U.S.A.) and Cogent Chipware (Vancouver, B.C.). She was on the Board of Directors of Mosaid Technologies (Ottawa, Canada) from 1997 to 2003.

She is author of the books, Semiconductor Memories (1982), Semiconductor Memories 2nd Edition (1992), High Performance Memories, (1996, revised 1999), Emerging Memories-Technologies and Trends, (2002), and Modern Memories to be published by John Wiley & Sons.

She is a Senior Member of the IEEE and is involved in the Non-Volatile Section of the ITRS Technology Roadmap. She was a member of the EIA JEDEC JC42 Memory Standards Committee for 20 years where she served as founder and chairman of the JC16 Electrical Interface Standards Committee, Co-Chair of the JC-42.4 SRAM/CAM Standards Committee and US National Delegate to the IEC SC47 WG3 International Memory Standards Group. She has served on the Editorial Board of the IEEE Spectrum, and has given technical papers and tutorials at various IEEE conferences. She holds several patents in the semiconductor memory area.

She has a B.Sc. in Physics, an M.Sc. in Physics, an MBA in International Business and a Ph.D. in International Finance.

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